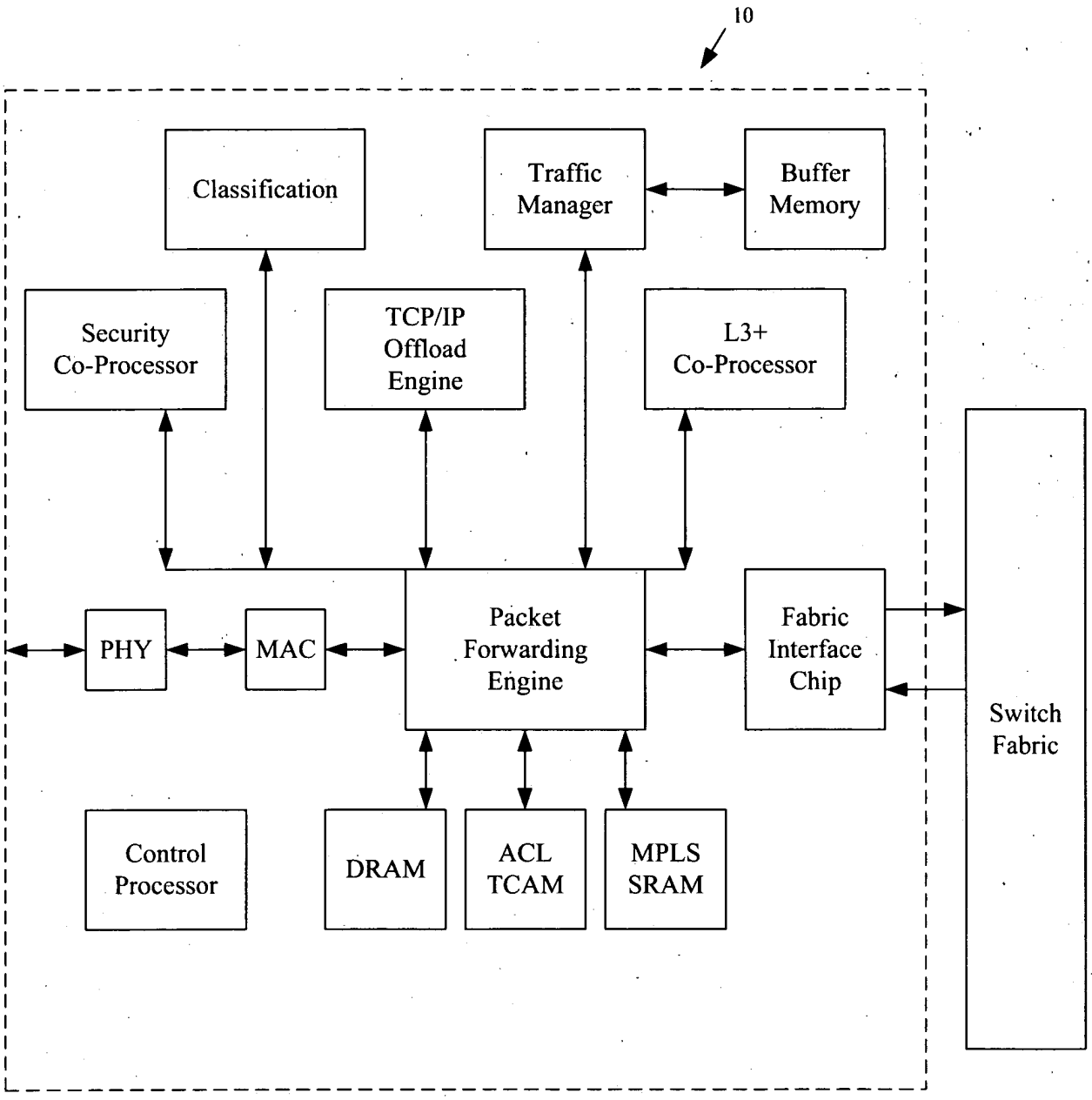

Figure 1
(Conventional)

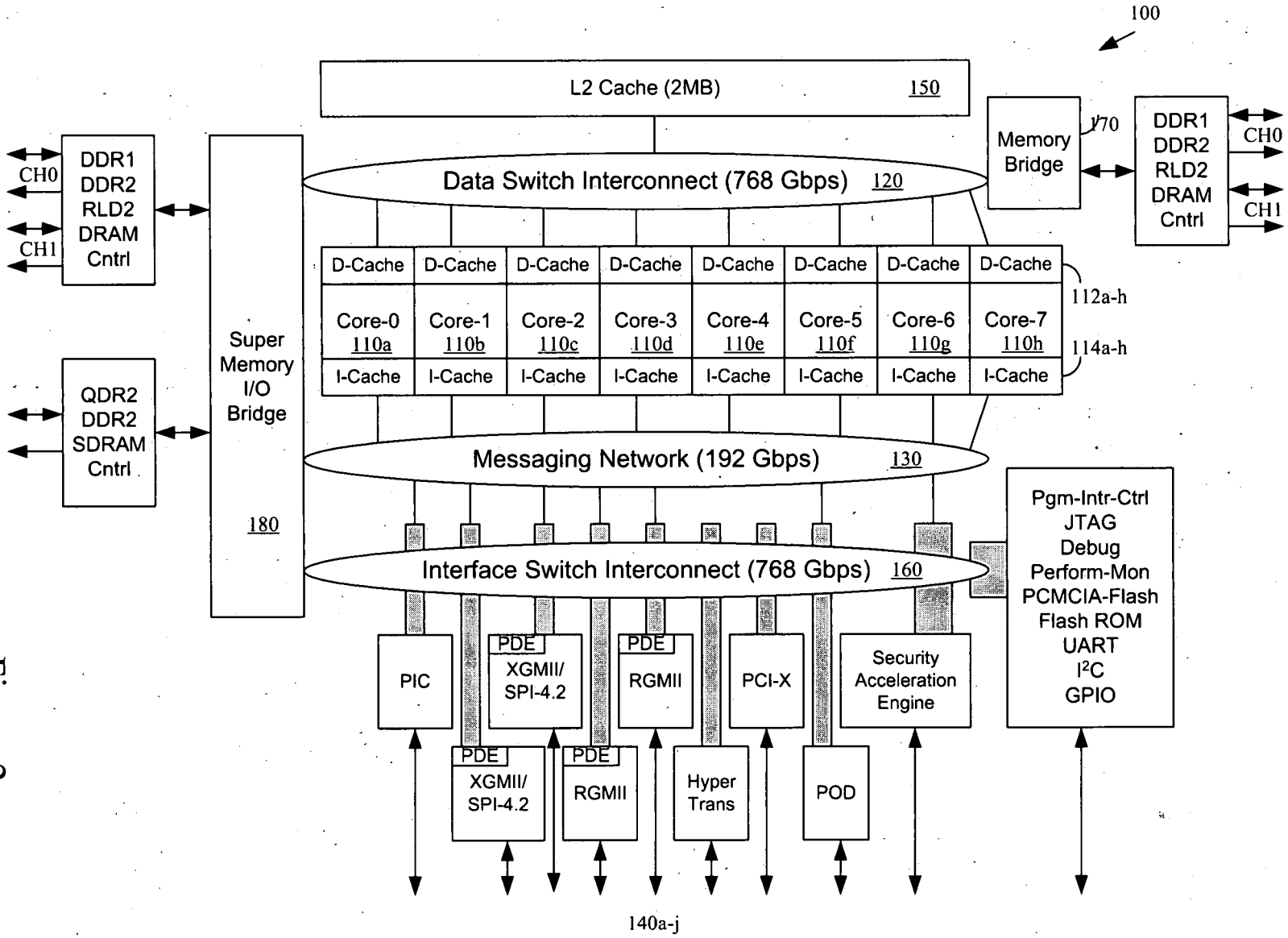
100
L2 Cache (2MB) 150
Data Switch Interconnect (768 Gbps) 120
Memory Bridge
170
DDR1 DDR2 RLD2 DRAM Cntrl
CH0
CH1
DDR1 DDR2 RLD2 DRAM Cntrl
CH0
CH1
Super Memory I/O Bridge
180
QDR2 DDR2 SDRAM Cntrl
D-Cache
Core-0 110a
Core-1 110b
Core-2 110c
Core-3 110d
Core-4 110e
Core-5 110f
Core-6 110g
Core-7 110h
I-Cache
112a-h
114a-h
Messaging Network (192 Gbps) 130
Interface Switch Interconnect (768 Gbps) 160
Pgm-Intr-Ctrl
JTAG
Debug
Perform-Mon
PCMCIA-Flash
Flash ROM
UART
I2C
GPIO
PIC
PDE
XGMII/ SPI-4.2
PDE
RGMII
PCI-X
Security Acceleration Engine
PDE
XGMII/ SPI-4.2
PDE
RGMII
Hyper Trans
POD
140a-j

Figure 2